

Applicant(s): Stephen J. Battersby et al.
Serial No.: 09/728,189
For: LIQUID CRYSTAL DISPLAY AND METHOD OF MANUFACTURE
Filed: December 01, 2000
Examiner: Akkapeddi, Prasad R.
Group Art Unit: 2871

REMARKS/ARGUMENTS

Claims 1 through 13 are pending in the present application.
Claim 4 has been amended.

The Action (1) rejected claims 1 to 4 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,759,610 to Yanagisawa ("the Yanagisawa patent"), (2) rejected claims 5 to 12 under 35 U.S.C. 103(a) as being as being unpatentable over the Yanagisawa patent in view of U.S. Patent No. 5,734,449 to Jang ("the Jang patent"), and (3) rejected claims 13 under 35 U.S.C. 103(a) as being as being unpatentable over the Yanagisawa patent in view of U.S. Patent No. 5,734,449 to Jang ("the Jang patent")

Regarding item (1) identified above, it is respectfully submitted that claim 1 is patentable over the Yanagisawa patent, and that claim 1 defines an invention that is neither disclosed nor suggested by the cited reference.

The Yanagisawa patent discloses an electrically conductive light shielding layer (28) formed on a transparent insulating substrate (16) so as to cover a TFT region before forming a TFT (11), a display pixel electrode (12) and a connecting portion (10). The Yanagisawa patent suggests that a silicon nitride film (29) serving as an insulating film be formed on the light shielding layer (28), that the TFT (11) and the display pixel electrode (12) be formed on the light shielding layer (28), and moreover, that the light shielding layer (28) be formed to overlap a part of the display pixel electrode (12) to form a

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supplemental storage capacitor. (col. 3, lines 41-49 and 59-63).

The Action contends the apparatus shown in Figs. 6 and 7, and more particularly Fig. 7, of the Yanagisawa patent discloses/suggests a "transistor having an insulated-gate staggered structure with substantially coplanar source and drain regions formed on [a] substrate" and a "capacitor associated with said transistor and lying adjacent thereto" (emphasis added).

In furtherance of the Response filed January 24, 2003, it is respectfully submitted that the above-identified contention is inconsistent with that which is taught by the Yanagisawa patent. That is, the Yanagisawa patent specifically teaches that an electrically conductive light shielding layer 28 is formed "on" a transparent insulating substrate 16 "so as to cover a TFT region before forming a TFT 11, a display pixel electrode 12 and a connecting portion 10" (emphasis added) (col. 3, lines 40-45).

This shielding requirement clearly teaches away from a "transistor having an insulated-gate staggered structure with substantially coplanar source and drain regions formed on [a] substrate", as defined by claim 1, at least in that it requires that TFT 11 be insulated from substrate 16. Furthermore, the Yanagisawa patent teaches/requires that another layer, a silicon nitride film 29, be used to insulate between the TFT 11 and the shielding layer 28. Hence, it is respectfully submitted that drain 20 and source 21, which form part of TFT 11, are not "on" substrate 16, but rather, are "above" substrate 16 and insulated therefrom via layer 28 and film 29.

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Thus, it is respectfully submitted that (1) the invention of present claim 1 is patentably distinct from that which is disclosed and/or suggested by the Yanagisawa patent, (2) the Yanagisawa patent fails to disclose all the elements defined by claim 1, and (3) the Yanagisawa patent teaches away from the invention defined by claim 1. Accordingly, adding the term "directly", as suggested in the Action, is an unnecessary limitation.

Moreover, and in furtherance of the foregoing, it is respectfully submitted that the Yanagisawa patent, contrary to that which is indicated by the Action, likewise fails to disclose or suggest a capacitor "lying adjacent" to a transistor. Rather, in clear contrast, the Yanagisawa patent teaches that shielding layer 28 be formed to overlap part of electrode 12 to form a supplemental storage capacitor, and that connecting portion 10 form a portion of this supplemental storage capacitor (col. 3, lines 60-65). Thus, since connecting portion 10, which is a small region connecting source 21 of TFT 11 and pixel electrode 12 (see Fig. 7), forms a part of the supplemental capacitor, the capacitor cannot lay "adjacent" to TFT 11, but rather is integrally connected therewith via connecting portion 10.

Accordingly, it is respectfully submitted, based at least on the foregoing discussion that claim 1 is patentable over the Yanagisawa patent. Thus, reconsideration and withdrawal of the rejection based on the Yanagisawa patent, and allowance of claim 1, are respectfully requested.

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Regarding claims 2 to 4, which depend either directly or indirectly from claim 1, it is respectfully submitted that they are each patentable at least for the reasons discussed above with respect to claim 1. Accordingly, reconsideration and withdrawal of the rejection, and allowance of claims 2 to 4, are respectfully requested.

Regarding item (2) identified above, it is respectfully submitted that claims 5 to 12 are patentable over both the Yanagisawa patent and the Jang patent, and that claims 5 to 12, which depend either directly or indirectly from claim 1, define an invention that is neither disclosed nor suggested by the cited reference combination.

The Jang patent is cited by the Action for disclosing a "relationship between the storage capacitance, liquid crystal material capacitance, thicknesses of the layers and the permittivity constants of the layers (Col. 3, lines 1-33)" (see p. 4 of the Action). It is respectfully submitted that irrespective of whether the Jang patent does in fact disclose the foregoing capacitance relationship, the Jang patent, like the Yanagisawa patent, fails to disclose or suggest "transistor having an insulated-gate staggered structure with substantially coplanar source and drain regions formed on [a] substrate" and a "capacitor associated with said transistor and lying adjacent thereto" (emphasis added).

Accordingly, it is respectfully submitted, based at least on the reasons discussed above with respect to claim 1 and the Yanagisawa patent, that claims 5 to 12 are patentable over the cited reference combination (i.e., the Yanagisawa patent and the

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Jang patent). Thus, reconsideration and withdrawal of the rejection based on such reference combination, and allowance of claims 5 to 12, are respectfully requested.

Regarding item (3) identified above, it is respectfully submitted that claim 13, which depends directly from claim 1, is patentable over both the Yanagisawa patent and the Jang patent for at least the same reasons identified/discussed above with respect to claim 1, and that claim 13 defines an invention that is neither disclosed nor suggested by the cited reference combination. Accordingly, reconsideration and withdrawal of the rejection based on such reference combination, and allowance of claim 13, are respectfully requested.

In sum, it is respectfully submitted that the pending claims are clearly patentable over each of the cited references and/or any proper combination thereof. Thus, this application is in condition for allowance. Accordingly, reconsideration and withdrawal of all rejections of the claims are respectfully requested.

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